CLAIMS

What is claimed is:

1. A method for obstructing access to a secure area of a semiconductor device comprising:

providing a control signal indicating that the semiconductor device has entered a secure mode; and

obstructing access to the secure area utilizing the control signal.

2. The method of Claim 1, wherein obstructing access to the secure area comprises gating another signal with the control signal.

3. The method of Claim 1, wherein obstructing access to the secure area comprises is selecting a multiplexer channel with the control signal.

4. The method of Claim 1, wherein obstructing access to the secure area comprises enabling another circuit with the control signal.

5. The method of Claim 1, wherein the secure area is used in connection with data encryption.

6. The method of Claim 1, wherein providing a control signal further comprises decoding a plurality of signals to generate the control signal.

7. The method of Claim 1, wherein the control signal transitions from a first logic state to a second logic state when the semiconductor device enters the secure mode.

8. The method of Claim 7, wherein the first logic state is a logic high and the second logic state is a logic low.

9. The method of Claim 7, wherein the first logic state is a logic low and the second logic state is a logic high.

10. The method of Claim 1, further comprising:

connecting an in-circuit emulator to the semiconductor device; and

generating a command from the in-circuit emulator to the semiconductor device, wherein the command requests access to the secure area of the semiconductor.

11. The method of Claim 10, wherein the semiconductor device enters the secure mode when the in-circuit emulator is connected to the semiconductor device.

12. The method of Claim 10, wherein the command is a software interrupt.

13. A system for obstructing access to a secure area of a semiconductor device comprising:

a first circuit for generating a control signal; and

a second circuit for obstructing access to the secure area connected to the control signal,

wherein the control signal is utilized by the second circuit to obstruct access to the secure area when a mode indicated by the control signal is a secure mode.

14. The system of Claim 13, wherein the second circuit is a logic gate.

15. The system of Claim 14, wherein the logic gate is an AND gate having

a first input connected to the first circuit such that the first input responds to the control signal;

a second input connected to a circuit supplying output data; and

an output connected to a port of the semiconductor device.

16. The system of Claim 13, wherein the second circuit is a multiplexer.

17. The system of Claim 13, further comprising a port for an in-circuit emulator.

18. The system of Claim 17, wherein the semiconductor device enters the secure mode when the in-circuit emulator is connected to the port.

19. The system of Claim 13, wherein the secure area comprises memory.

20. The system of Claim 13, wherein the semiconductor device is an application specific integrated circuit.

21. The system of Claim 20, wherein the first circuit is a microprocessor core.

22. They system of Claim 13, wherein the first circuit is a decoder.

23. The system of Claim 15, wherein the output is buffered before connecting to the port.

24. A system for obstructing access to a secure area of a semiconductor device comprising:

a microprocessor core;

a decoder connected to an output of the microprocessor core;

a control line connected to an output of the decoder;

a circuit for supplying output data;

a data output line connected to an output of the circuit for supplying output data; and

an AND gate having a first input connected to the control line, a second input connected to the data output line, and an output connected to an input of a buffer; and

a port implemented in the semiconductor device for connecting to an in-circuit emulator, wherein a line on the port is also connected to an output of the buffer,

wherein when the in-circuit emulator requests access to the secure area, the microprocessor core generates microprocessor signals for decoding by the decoder, and

wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and

wherein the AND gate outputs an obstructing signal to obstruct access by the in-circuit emulator to the secure area.